

final report

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Modular and Wireless Control System for SmartStim System

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Executive summary

The current project proposes to develop the hardware and software to support Smart Stimulation systems. The proposed solution involves the development of a modular, custom tailored system that makes extensive use of advanced wireless, micro controller and Digital Signal Processing (DSP) technologies. This architecture that will allow for scalability, encourage distribution of intelligence, reduce cost and encourage flexibility.

The following components were designed and developed as follows:

i) Development of model for the conceptual system architecture

The draft architecture of the control system under development is complete. This concept forms the platform for subsequent software development.

The proprietary algorithm was successfully implemented on a DSP (Digital Signal Processing) platform. The software application for the wireless development kit was implemented and wireless communication was established and demonstrated simulating a Master/Slave scenario.

ii) Modeling carcass responses and associated algorithm

An extension was requested for Milestone 2 reporting due to an unexpected delay in the delivery of the TMS320F28335 development kit. In the meantime, to compensate for the delay, a significant amount of work was directed at prototype design. As a result, the design of wireless printed circuit board (PCB) for the ZigBee Module & ZigBee Relay is now complete. The PCB has been manufactured and is now ready for assembly and testing. This will enable delivery of the 3rd milestone on time.

iii) Controller Development

Data acquisition was tested using the *TMDSDOCK28335 Experimenter Kit*. The design of wireless printed circuit board (PCB) for the ZigBee Module & ZigBee Relay is now complete. These have been assembled and tested for functionality. Further tests will be carried out in a simulated environment for power, range and reliability. The system motherboard design is underway

iv) Software Development

The software for the system functional blocks was developed as separate software modules and tested on three development platforms. The modules include:

- Data Acquisition
- Proprietary algorithm implementation
- Serial communication
- Wireless communication

Simulations were mainly carried out on acquired load cell data and dummy data to prove the concept and assess the hardware requirements. The information obtained from these simulations was used to select the devices [electronic components] for the system motherboard and related hardware. Having tested these modules separately, they can now be integrated to develop the complete system software. Similarly, the hardware components developed to date can now be integrated in order to design and develop the system motherboard and wireless communication system.

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1 Background

Meat and Wool New Zealand and Meat and Livestock Australia have jointly funded the development of a technology that measures the responses of each carcass to the stimulation. This technology has been termed SmartStim, because it allows the response characteristics from each carcass to be analysed and subsequent stimulation tailored to the need of that carcass. SmartStim is expected to develop into an on-line real time quality measurement and control system that will form the basis for the next generation of electrical stimulation equipment.

The development of the SmartStim system is reaching a point where the final commercial configuration of the system needs to be confirmed. For the commercial trials of the system, a PC-based software control was developed and has proved to be adequate for this purpose. Indeed, this could be an acceptable platform for the SmartStim system, and Merit of Measurement are currently upgrading the LabView SmartStim software for the on-going work, and the software engineer doing this has been directly involved in the development of the system for the last two years.

The limitation of this approach is that PCs are generally recognised as having limitations in harsh environments. Carne Technologies and Merit of Measurements (MoM) evaluated, as an alternative, the option of using Programmable Automation controllers (PACs). The most appropriate is the National Instruments CompacRIO that can run the existing LabView programme developed for the SmartStim application. Although robust, powerful and versatile, this approach has limitations that have significant impact on flexibility and cost. In particular:

- Although modular, the amount of flexibility available between various configurations is limited by the actual structure of each module, e.g. a module with 4 load cell inputs needs to be purchased even if only one channel needs to be recorded.
- As it attempts to be everything to everybody, the CompactRIO system features far more processing and computing capability than it will ever be required for this particular application. Whether it is used or not, this capability is factored in the purchase price.
- Due to the high cost, the only configuration that makes sense is to have only one controller for each installation, regardless of the number of load cell and stimulations stations. It shall not be possible then to locate the controller in the immediate vicinity of all the load cells. Consequently a significant amount of wiring shall be required in most installations, resulting in:
 - Increased installation complexity and cost;
 - Decreased electrical signal quality;
 - The introduction of more potential sources of hardware failure.
- The introduction of new features will be constrained by the interfacing capabilities that the platform offers at each point in time.
- The owner of the IP incorporated in the SmartStim system has no control over the type and characteristics of the hardware components or the software development tools that shall be available from the manufacturer in the future.
- The design of the system will end up being a compromise between the requirements of the SmartStim process and the control equipment's features and capabilities, rather than being developed from the ground up so that it completely fulfils the current requirements and allows for future enhancements.

Purpose and Description

The proposed solution involves the development of a modular, custom tailored system that

makes extensive use of advanced wireless, micro controller and Digital Signal Processing (DSP) technologies. This architecture that will allow for scalability, encourage distribution of intelligence, reduce cost and encourage flexibility.

The following hardware components of a control system shall be developed as part of the project:

- 1. Primary Controller:
- It shall be part of any configuration, regardless of the number of load cell stations required;
- It shall always be located at the first load cell station along the chain;
- Features and capabilities: everything that is listed under the *Functional requirements* bullet point list on page 1 above.
- 2. Secondary Controller:
- It shall be part of all the configurations that feature more than one load cell station;
- There shall be one secondary controller per each load cell after the first one.
- Features and capabilities: identical with the Primary Controller, except that it will NOT feature:
 - a. Storing the results on board for subsequent remote data retrieval;
 - b. Sending stored data to the meat plant information system using a built-in ftp server;
 - c. Allowing remote monitoring and control using a built-in web server.
- 3. Digital Control Slave Unit:
- Shall be incorporated into the electrical stimulus generator unit and attached to the stimulation bars, if they are present in the configuration.
- Shall receive a digital signal from the associated controller over the wireless network and shall convert it into an electrical signal that in turn will trigger electrical stimulation of the carcass.

Wherever possible, the hardware components shall be developed by leveraging existing boards and circuits available in the market (e.g. wireless communication modules) rather than developing from component level up.

Advantages:

- Highly modular, fully configurable architecture: each system will feature only those components that are actually required;
- Due to the small size of the controller, it shall be possible to locate it very close to the load cell, allowing for a very good quality signal to be recorded without any additional signal conditioning;
- The wireless capability will drastically reduce the amount of wiring required. The installation process will be quick and simple.
- Because the controller will contain only those components that are actually required for its proper functioning, the cost will be significantly reduced, from a minimum of \$5450 with the cRIO option, to an estimated \$500 for the custom tailored option.

Disadvantages:

• It is yet to be made.

To develop the hardware system, Merit of Measurement is proposing the following steps.

- The development of the system will be carried out as a Master's of Engineering project by a student enrolled at the Auckland University of Technology. The student will be part of the School of Engineering, Electrical and Electronic Engineering Department which has specific expertise in wireless communication.
- The student has been identified: he carried out his undergraduate work at AUT and at Latrobe University in Melbourne and is currently working in industry.
- The project will be carried out with Merit of Measurement under the mentorship of Mihai Costache, Managing Director.
- A key aspect of the proposed project is to use, wherever possible, existing components and circuits that are already available 'off the shelf'. These will be integrated with the new developments required for this specific application to develop a complete system. This strategy will produce the most cost-effective and timely development process.
- The work is expected to require 1 year.

Industry Benefit / Impact

The overall benefit of development of a systems controller unit will allow commercialisers of Smart Stim and other compatible technologies to offer alternative controller options with more robust data capture capabilities. This proposed Phase 1 will develop a commercial prototype controller unit that will be tested and evaluated in pilot environment. At the conclusion of this proposed Phase 1 work, the option for a Phase 2 commercial trials will be reviewed. The outcomes of this project will be delivered to commercialisers of SmartStim and similar technologies where data capture and data protection is required.

2 Project Outline

The following are the milestones:

Final Report

A final report will be completed that will define the performance characteristics of the controller and its suitability for commercialising the SmartStim system. A ME Thesis will be submitted to Auckland University of Technology.

New Technology

The SmartStim controller will represent the new technology produced from this project.

Commercialisation/Dissemination Strategy

The commercialisation strategy for the controller will be incorporated into the overall strategy for commercialising the SmartStim technology, currently under development within the MQST program.

3 Project Objectives

The project objective was develop and validate a purpose-designed control system for SmartStim that will form the platform for the commercialisation of the technology.

4 Experimental work

The following were the milestones:

1. Development of model for the conceptual system architecture: evaluate available off the shelf solutions for DSP and wireless technologies; build system blocks and integrate these blocks to represent a functional system

2. Modelling carcass responses and associated algorithm: Develop a Simulink Model of the system architecture based on the building blocks for the modelled architecture in Milestone 1; Present a working simulation of the system that will be used carcass response signals and communication scenarios

3. Controller Development: Finalize system blocks and choose system platform; start building system on development board and validate functional blocks. Software development; Demonstrate a working prototype to prove concept

4. System realizing and testing: Design a test and validation plan; Measure system performance as per agreed specification. Present to Commercialiser(s) of Smart Stimulation in Australia & NZ and pilot plants

5 Results & Discussion

5.1 Development of model for the conceptual system architecture: Evaluate available offthe-shelf solutions for DSP and wireless technologies; Build system blocks and integrate these blocks to represent a functional system

The overall system architecture, as well as the architecture of the control system under development have been defined and specified. Using a development kit, it was proven that the same results can be obtained while processing acquired data on a DSP, as that previously obtained in the field during trials. Several options for hardware components and corresponding development tools have been evaluated. A wireless development kit has been purchased and is currently trialed.

The project was initiated by clearly defining the problem at hand through meetings with the client, and with the engineer who developed the previous PC software application for the SmartStim pilot installations. The complete SmartStim system specification was characterized and the functional aspects were fully understood through exchange of information with the client and the developer.

The overall system architecture (see Schematic 1) is shown below:



Schematic 1 - overall system architecture

Ongoing literature review confirms that the proposed system in this project is unique and the technology behind measurement and control of carcass pH through electrical stimulation is currently unavailable elsewhere.

Raw data acquired from the pilot installations was supplied by the client and formed the basis for developing the conceptual system and simulation. The raw data was analyzed using mathematical software [MATLAB] by implementing a proprietary algorithm. The same algorithm was then implemented on Texas Instrument DSP 6713 starter kit platform and the results obtained were identical to that obtained by MATLAB.

Several options have been considered and evaluated during the selection process for the microcontroller [MCU], the digital signal processing [DSP] device and the ZigBee processor. The associated tools e.g. code compilers and emulators, have also been considered in the process.

The most suitable DSP device will be selected after completing further analysis of each available device's capabilities vs. algorithm computing requirements. This work involves evaluating the results obtained while using Radix2, Radix4 and mixed Radix Fast Fourier Transforms [FFT] to identify the most suitable FFT for this application. The most important factor considered is the number of processor cycles required for each FFT to process 1500 data points.

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ZigBee has been confirmed as the preferred low power wireless communication protocol for this project. Evaluation of available devices and defining the ZigBee based system communication protocol is currently underway. A Texas Instruments ZigBee eZ430 development kit has been purchased and is currently trialed. Work is also under way to establish the wireless communication protocols for the system.

The draft architecture of the control system under development is complete. This concept forms the platform for subsequent software development. The architecture of the control system is depicted below (see Schematic 2):



Schematic 2 - The draft architecture of the control system

5.2 Modeling carcass responses and associated algorithm.

Develop a Simulink Model of the system architecture based on the building blocks for the modeled architecture in Milestone 1. Present a working simulation of the system that will be used for carcass response signals and communication scenarios.

The architecture of the control system under development is complete. This concept forms the platform for subsequent software and hardware development.

The proposed system software architecture has also been completed.

The proprietary algorithm was successfully implemented on a DSP (Digital Signal Processing) platform.

The software application for the wireless development kit was implemented and wireless communication was established and demonstrated simulating a Master/Slave scenario.

The architecture of the overall control system under development is now complete. This concept forms the platform for subsequent software and hardware development.



Figure 1 – Overall Control System Architecture

The proposed system software architecture has also been completed. The system software is developed according to this architecture and shall be optimized once the hardware prototype is available.



Figure 2 System Software Architecture

The proprietary SmartStim algorithm was successfully implemented on a DSP (Digital Signal Processing) platform, namely Texas Instruments TI DSK 6713. Using the RADIX2 Fast Fourier Transform algorithm, the results obtained from the DSP platform were same as the results calculated through simulation in MATLAB. Utilizing the Texas Instruments optimized DSP Library, the total time taken to perform a 1536 point FFT is detailed below.

Cycles: (2 * n * log (base-2) n) + 42

n = 512, Cycles = 9258

If the DSP clock is running at 100MHz then computation time is 92.6µs. By processing the points in blocks of 512 at a time, the total computation time is 278µs. The RADIX2 FFT algorithm proved to be adequate for this application. Further real time analysis is required to confirm the limitation of the system in terms of maximum allowable carcass transport speed, reliability of carcass detection and Master/Slave synchronization. These will be fully tested and verified once the 1st prototype is ready.



Figure 3. Simulation result in MATLAB

The Texas Instruments TMS320F28335 DSP/MCU device has been selected for this application. Several of these devices have been purchased for the 1st prototype.

The ZigBee application was developed and wireless communication was established and demonstrated simulating a Master/Slave scenario. Successful exchange of data and commands was established using the eZ430-RF2480 kit.

A 4 node network was set up to simulate Master/Slave and Master/Relay configurations. Commands and messages have been successfully transmitted and received between the various units. During the demonstration it was possible to turn remote relays on/off and to receive dummy pH values from the slave units at regular intervals.



Figure 4 Master Controller [AVR ATmega 8535]



Figure 5 Slaves on eZ430-RF2480

5.3 Controller Development

Finalize system blocks and choose system platform. Start building system on development board and validate functional blocks. Develop software and demonstrate a working prototype to prove concept.

The system blocks have been finalized and the hardware platform chosen. The software was developed as functional units and tested to prove the concept. The system motherboard which is currently under development will allow for the full integration of the software and hardware components into the complete purpose-designed control system for the SmartStim application.

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Figure 6 - TMDSDOCK28335 Development Platform and C2000 emulator

The Texas Instruments TMS320F28335 digital signal controller from the C2000 family has been selected for this application. Several of these devices have been purchased for the 1st prototype. This is a floating point microcontroller that operates at up to 150MHz and offers up to 300 MFLOPS and 512KB of on-chip flash memory. Other applications for this device in various industries include digital motor control, digital power supply and advanced sensing in industrial, automotive, medical and consumer markets.

The analogue-to-digital converter (ADC) was configured to run in continuous mode, converting the input at channel A0 and logging it in the *SampleTable* buffer. The ADC clock was set at its maximum value of 12.5MHz, giving a maximum sampling frequency of 781.25 kHz. The maximum frequency component of the carcass stimulus response is approximately 500Hz. Therefore the sampling frequency of our data acquisition block should be at least 1 kHz. Further tests shall include sampling at different (higher) rates, using external triggers to start conversion and investigation of ADC offset effects on input signal acquisition (offset error).

A function / arbitrary waveform generator has been purchased. This was used to simulate load cell response and setup event triggers for events such as carcass on load cell and start / end of stimulation pulses.

SampleTable						-
0x0000C040	SampleTa	able				×
0x0000C040	0x042D	0x042D	0x042C	0x042D	0x042D	±
0x0000C045	0x042D	0x042C	0x042D	0x042C	0x042D	-
0x0000C04A	0x042D	0x042C	0x042D	0x042D	0x042E	
0x0000C04F	0x042D	0x042C	0x042D	0x042D	0x042E	
0x0000C054	0x042E	0x042D	0x042C	0x042D	0x042E	
0x0000C059	0x042C	0x042C	0x042D	0x042D	0x042D	
0x0000C05E	0x042D	0x042D	0x042E	0x042D	0x042D	
0x0000C063	0x042D	0x042D	0x042D	0x042D	0x042D	
0x0000C068	0x042D	0x042D	0x042D	0x042D	0x042D	
0x0000C06D	0x042C	0x042E	0x042D	0x042D	0x042D	
0x0000C072	0x042D	0x042C	0x042C	0x042E	0x042E	
0x0000C077	0x042D	0x042D	0x042D	0x042D	0x042D	
0x0000C07C	0x042E	0x042D	0x042D	0x042C	0x042D	
0x0000C081	0x042D	0x042D	0x042C	0x042D	0x042D	
0x0000C086	0x042C	0x042D	0x042D	0x042D	0x042D	
0x0000C08B	0x042E	0x042D	0x042D	0x042D	0x042D	
0x0000C090	0x042D	0x042D	0x042E	0x042C	0x042D	
0x0000C095	0x042D	0x042D	0x042D	0x042D	0x042E	-1
0x0000C09A	0x042E	0x042D	0x042D	0x042E	0x042C	-
0x0000C09F	0x042E	0x042D	0x042C	0x042D	0x042D	Ŧ
0v00000034	0.0420	0v042D	0.0420	0v042D	0v042D	T
🖌 🔳 Hex 1	6 Bit - 💌	Data 💌				

Figure 7 - Data Acquisition simulation: Buffer contents

Name	Value	Туре	Radix
🗆 🔗 SampleTable	0x0000C040	unsigned int[2048]	hex
[0]	1069	Uint16	unsigned
[1]	1069	Uint16	unsigned
[2]	1068	Uint16	unsigned
[3]	1069	Uint16	unsigned
[4]	1069	Uint16	unsigned
§ [5]	1069	Uint16	unsigned
(6)	1068	Uint16	unsigned
[7]	1069	Uint16	unsigned
[8]	1068	Uint16	unsigned
(9)	1069	Uint16	unsigned
[10]	1069	Uint16	unsigned
[11]	1068	Uint16	unsigned
[12]	1069	Uint16	unsigned
(13)	1069	Uint16	unsigned
	1070	Uint16	unsigned
I 15	1069	Uint16	unsigned

33x\v120\DSP2833x_examples\adc_seqmode_test\Example_2833xAdcSeqModeTest.c

Figure 8 - ADC Channel A0 Log of converted values

The digital value of the input voltage is derived by:

Digital Value = 0,

Ln 170, Col 1

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Digital Value = 4096 x Input Analog Voltage – ADCLO 3 Digital Value = 4095, when input $\ge 3V$

The development of the ZigBee application and the testing of the wireless communication on the eZ430-RF2480 development kit were reported at the completion of milestone 2.

During this current milestone, the ZigBee components have been tested in conjunction with the ADC.

Figure 4 below shows the commands and messages sent wirelessly. These were captured using Packet Sniffer. The frame segment APS Payload shows the actual data sent. In these segments APS Payload = 07 represents the dummy pH value, while APS Payload = 01 is the "Relay ON" command.



Figure 9 - Over-the-air packet capture using Packet Sniffer

The Texas Instruments CC2480 processor has been selected to handle the wireless communication. The CC2480 is the first product from the new Z-Accel family of ZigBee-certified network processors. Z-Accel makes it easy to add ZigBee functionality to new or existing applications and allows the flexibility to work with any microcontroller unit (MCU).

A circuit board was designed for the ZigBee devices. Twenty-four such boards were manufactured, allowing for several trials to be carried out during the last milestone for optimisation purposes.



Figure 10 - Bare ZigBee PCB: Bottom Layer



Figure 11 - Bare ZigBee PCB: Top Layer

The wireless communication application software on eZ430-RF2480 kit will now be ported to the newly designed CC2480 ZigBee boards as shown in *Figure 7* and *Figure 8* below. Preliminary ii) *Modeling carcass responses and associated algorithm* RF tests have shown that these boards are functional.



Figure 12 - CC2480 and 2.4GHz PCB Antenna



Figure 13 - Host MCU: AVR ATtiny88

The system motherboard preliminary design has commenced, allowing for suitable devices to be selected in order to fulfill the overall system specifications. The main components of the motherboard are

- Power supply: 12V, 5V, 3.3V
- System Controller
- Data Acquisition Module
- Wireless Module
- Serial Communication Module



Figure 14 - System motherboard design - stage 1 (MoM: Altium PcbDoc file)

6 Project Outcomes

i) Development of model for the conceptual system architecture

The draft architecture of the control system under development is complete. This concept forms the platform for subsequent software development.

ii) Modeling carcass responses and associated algorithm

An extension was requested for Milestone 2 reporting due to an unexpected delay in the delivery of the TMS320F28335 development kit. In the meantime, to compensate for the delay, a significant amount of work was directed at prototype design. As a result, the design of wireless printed circuit board (PCB) for the ZigBee Module & ZigBee Relay is now complete. The PCB has been manufactured and is now ready for assembly and testing. This will enable delivery of the 3rd milestone on time.

iii) Controller Development

Data acquisition was tested using the *TMDSDOCK28335 Experimenter Kit*. The design of wireless printed circuit board (PCB) for the ZigBee Module & ZigBee Relay is now complete. These have been assembled and tested for functionality. Further tests will be carried out in a simulated environment for power, range and reliability. The system motherboard design is underway

7 Conclusion

The software for the system functional blocks was developed as separate software modules and tested on three development platforms. The modules include:

- Data Acquisition
- Proprietary algorithm implementation
- Serial communication
- Wireless communication

Simulations were mainly carried out on acquired load cell data and dummy data to prove the concept and assess the hardware requirements. The information obtained from these simulations was used to select the devices [electronic components] for the system motherboard and related hardware. Having tested these modules separately, they can now be integrated to develop the complete system software. Similarly, the hardware components developed to date can now be integrated in order to design and develop the system motherboard and wireless communication system.

9 Acknowledgements

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